iEnergy

ARTICLE

https://doi.org/10.23919/IEN.2022.0033

Low-voltage ride through of multi-port power electronic transformer

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ABSTRACT

A low-voltage ride-through (LVRT) control strategy for the multi-port power electronic transformer (PET) based on power co-regulation is proposed. During the sag and recovery of the grid-side voltage of the medium-voltage ac (MVac) port, the grid-connected active power of the low-voltage ac (LVac) port, rather than the power from external renewable energy sources (e.g., photovoltaic (PV)), is adjusted quickly to rebalance the power flowing across all ports, thereby preventing overcurrent and overvoltage. Moreover, a power-coordinate-frame-based LVRT mode classification is designed, and a total of six LVRT modes are classified to meet the LVRT requirements in all power configuration scenarios of the PET. In this way, the PET is endowed with the LVRT capability in both power-generation and power-consumption states, which is significantly different from traditional power generation systems such as PV or wind power. Furthermore, by optimizing the active power regulation path during LVRT transition, the overcurrent problem caused by the grid-voltage sag-depth detection delay is overcome. Finally, the effectiveness of the proposed control scheme is verified by experiments on a hardware-in-the-loop platform.

KEYWORDS

Active-power regulation path optimization, low-voltage ride through (LVRT), LVRT mode classification, power electronic transformer (PET).

Distributed energy resources (DERs), e.g., wind power and photovoltaic (PV), have become more important recently in order to reduce fossil fuel usage and CO_2 emission. As an increasing number of DERs are connected to the grid through interface converters, their dynamic behaviors are critical to the stability of power systems. Many grid codes[1,2] are released to guide their operation, and it is now mandatory for PV and wind-power systems to ride through temporary low-voltage grid faults, known as the low-voltage ride-through (LVRT) capability. In the LVRT process, DERs should remain connected and support the grid by injecting reactive and active power[3,4]. Moreover, with the application of multi-port power electronic transformer (PET), the structure of the distributed energy system has been reorganized and simplified, and the LVRT of multi-port PET becomes an inevitable and novel research topic, which is quite different from the traditional one.

For the traditional LVRT of PV[5–11] or wind-power system[12,13], many studies have been carried out in the past based on advanced control strategies. The vector current controller with feedforward (VCCF) of negative-sequence grid voltage and dual vector current controllers (DVCCs) can produce the required current to meet the LVRT requirements. But the unbalanced and dropped grid voltages may easily lead to excessively high current stress on the grid-connected converter[5]. In order to avoid the overcurrent protection, a new control method with a predefined ampere constraint is proposed in ref. [6]. It has the unique advantage of offering greater flexibility in the combination of positive- and negative-sequence currents, therefore achieving the desired grid-voltage compensation in terms of voltage quality support or imbalance mitigation. However, the limitation of the second-order ripple in the dc-link voltage is not considered in this solution. In ref. [7], a novel adaptive dc-link voltage control method for the two-stage PV inverter is introduced to achieve balanced sinusoidal currents and limit the dc-link voltage ripple in asymmetrical voltage dips. In ref. [8], a multi-objective control strategy involving reference current determination and scenario classification is presented. It can realize three objectives, i.e., grid voltage support, ac output current limitation, and dc-link voltage ripple suppression, during all voltage sag scenarios. Moreover, Tang et al. present an improved multi-mode control strategy for the three-phase PV power system with LVRT capability[9]. An islanding detection and LVRT solution of a two-stage PV inverter are proposed and verified in ref. [10]. The LVRT methods for converters using droop control in microgrids are studied in refs. [13] and [14].

The detection duration of the grid-voltage sag depth is also strictly limited by the grid code[2], and it is mandatory to be detected as quickly and accurately as possible so that the grid-connected converter can respond correctly in time, thereby achieving low-oltage ride through. In ref. [15], a fast amplitude estimation (FAE) method without PLL structure is proposed. It has fast dynamics and can be a promising solution for single-phase systems, but has poor immunity to harmonics. Ref. [16] presents a detection method with the maximum-point and the zero-point tracking algorithm. Its transition time is about 10 ms, but the logic judgment is complicated. Furthermore, the comparison results[16] show that the response time of PLL-based methods is much greater than 10 ms. Therefore, the grid-voltage sag-depth detection needs to be further improved.

The LVRT control strategies above are usually only suitable for two-stage grid-connected converters and unidirectional power

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flow scenarios in traditional distributed energy systems, where each individual PV or wind-power system needs to be given the LVRT capability. Fortunately, by integrating PV converters, energy storage systems, and wind-power systems into a multi-port PET, the entire configuration of the distributed energy system can be reorganized[17], as shown in Figure 1. In this case, only the medium-voltage ac (MVac) port, not each individual DER converter, needs to have the ability to ride through grid faults, while the voltage quality of DER converters can be maintained by the PET. However, considering the complexity of the power flow within the PET, which is quite different from traditional PV and wind power systems, the LVRT control for the multi-port PET is more complicated. Therefore, it is of great significance to research on this topic, which is still very limited until now.

This paper presents a comprehensive control strategy for a multi-port PET, and the ability to ride through medium-voltage dc (MVdc) grid faults is realized. Section 1 introduces the proposed LVRT control scheme. Both in power-generation and power-consumption states of the MVdc port, the PET has LVRT capability. In Section 2, the LVRT mode classification is discussed. Six LVRT modes are presented according to different scenarios. In Section 3, the grid-voltage sag-depth detection method is described. In Section 4, an active-power regulation path optimization method is presented to improve the dynamic performance during the LVRT transition. Section 5 gives the control implementation and control parameter determination. The experimental results are provided in Section 6. Finally, conclusions are summarized in Section 7.

1 LVRT scheme for the multi-port PET

As shown in Figure 1, the high-frequency-bus-based PET (HFB–PET) is implemented in refs. [17] and [18] to provide four ports, that is, a MVac port connected to the MVac-distribution grid with a star-configuration, a low-voltage ac (LVac) port with the three-phase three-wire condition, a low-voltage dc (LVdc) port, and a MVdc port. In this paper, the LVRT control of this PET is elaborated, and it can be extended to the PET with more ports.

Figure 1 shows an operation scheme in the data center. The LVac port is connected to the LVac grid. PV arrays and energy storage systems are connected to the MVdc and LVdc ports through dc/dc converters independent of the PET. dc and ac loads are installed on the LVdc and LVac ports, respectively. Under this configuration, the operation modes of the four ports are set as follows.

(a) Grid-forming (constant-voltage) mode for the MVdc and LVdc ports.
(b) P/Q mode for the LVac port.
(c) Grid following mode for the MVac port. That is, the active power of MVac port is controlled to follow that of other ports, so as to achieve power balance among all ports.

In particular, the MVac port plays a crucial role in this scheme. Except for P/Q four-quadrant operation capability, it is also responsible for strengthening the stability of HFB. Once it fails, the voltages of HFB cannot be maintained, and other ports will be blocked. Therefore, the LVRT control of MVac port is a critical issue that will be focused on in this paper.

1.1 LVRT requirements

When the grid voltage of the MVac port drops, the LVRT requirements of the multi-port PET are specified as follows.

(a) The MVac port will not only keep the grid-connected operation but also support the grid by reactive power injection, and its active power can be quickly restored after the grid fault is cleared.
(b) Other ports can continue to operate normally and avoid load shedding as much as possible.
(c) The PET should have the LVRT capability both in power-generation and power-consumption states of the MVac port.

The first item mentioned above is consistent with the LVRT requirements of traditional PV systems. The latter two are special requirements for the multi-port PET.

1.2 LVRT scheme

When a voltage sag occurs on the grid side of the MVac port, the active power of other ports needs to be adjusted to realize power rebalance among all ports and prevent overcurrent. Three potential schemes are listed as follows.

Scheme-1: adjusting the output power of the PV array by controlling the external dc/dc converter shown in Figure 1. This solution is essentially the same as that for the traditional LVRT in PV or wind-power applications. However, it is not suitable for the power-consumption state of MVAC port, as the PV output power can't be further increased to compensate for the active-power

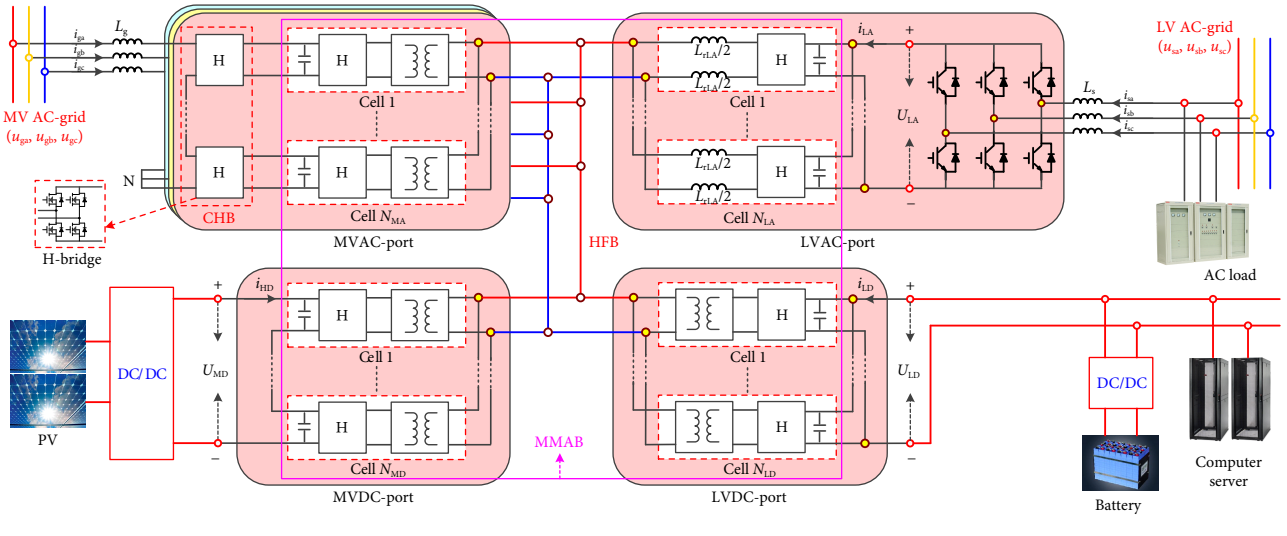

Fig. 1 Four-port high-frequency-bus-based PET used in the data center.

reduction from the MVac grid when the grid voltage drops. Moreover, the dc/dc converter, as an external device of PET, is not conveniently controlled.

Scheme-2: adjusting the active power flowing in the dc port after changing its operation mode from constant voltage to constant power. Under this scheme, the operation mode of the external dc/dc converter also needs to be changed. Thus, the control strategy is more complicated than that of *Scheme-1*.

Scheme-3: adjusting the active power exchanged between the LVac port and the LVac grid.

In comparison, *Scheme-3* does not need to change the operation mode of each port and can be easily implemented without PV output-power adjustment. It is especially suitable for the situation where the control of the PV converter is independent of the PET. In addition, it can be well applied to both power-generation and power-consumption modes of the MVac port. Therefore, *Scheme-3* is adopted in this paper.

2 LVRT mode classification of the multi-port PET

Regardless of the imbalance problem, the grid-voltage sag depth is defined as

$$N_v = U_{gm} / U_{gm(rated)} \tag{1}$$

where U_{gm} and $U_{gm(rated)}$ are the measured and rated amplitude of the grid voltage, respectively.

According to the newly released Chinese grid code[2], the MVac port will enter into the LVRT mode from the normal operation mode once the grid-voltage sag depth N_v is less than 0.9. With respect to the grid-voltage support, the injected reactive current and reactive power are defined as

$$\begin{cases} I_Q = 1.5 \times (0.9 - N_v) I_{m(rated)} & 0.2 \leqslant N_v \leqslant 0.9 \\ I_Q = 1.05 \times I_{m(rated)} & N_v < 0.2 \\ I_Q = 0 & N_v > 0.9 \end{cases} \tag{2}$$

$$Q_{MA} = -3U_{gm} I_Q / 2 \tag{3}$$

where $I_{m(rated)}$ is the rated current amplitude of MVac port[2].

In order to prevent overcurrent protection, there must be a limit on the active current. The maximum active current and power that can be tolerated by the MVac port are determined as

$$|I_{P(max)}| = \begin{cases} \sqrt{I_{m(rated)}{}^2 - I_Q{}^2} & 0.234 < N_v \leqslant 0.9 \\ 0 & N_v \leqslant 0.234 \\ I_{m(rated)} & N_v > 0.9 \end{cases} \tag{4}$$

$$P_{MA(max)} = 3U_{gm} I_{P(max)} / 2 \tag{5}$$

where $I_{P(max)} < 0$ when the MVac port is working in the power-generation state, and $I_{P(max)} > 0$ in power-consumption state.

Furthermore, without considering the power loss of the PET, the active-power balance among all ports should be maintained.

$$P_{MA} + P_{MD} + P_{LD} + P_{LA} = 0 \tag{6}$$

where P_{MA}, P_{MD}, P_{LD}, and P_{LA} respectively represent the input active power of MVac, MVdc, LVdc, and LVac ports.

The active-power configurations of the multi-port PET can be divided into six scenarios illustrated as *Case-1* to *Case-6* in Figures 2 and 3, where the horizontal and vertical axes represent P_{LA} and P_{MA}, respectively. The operating point of PET at any time must follow the power-balance line which is defined in Eq. (6). The powers of LVac and MVac ports are constrained by the rated active power $|P_{LA(rated)}|$ and $P_{MA(max)}$ defined in Eq. (5), respectively.

Subsequently, the LVRT mode of the PET can be classified according to the active-power configurations, shown in Figures 2 and 3, and the voltage sag depth N_v.

2.1 LVRT modes in the power-generation state

In the power-generation state (i.e., $P_{MA} < 0$), the MVac port should provide reactive-power support and deliver as much active power as possible to the grid during the LVRT period[9]. As shown in Figure 2, the LVRT modes can be divided into *Mode-1*—maximum active current, *Mode-2*—limited active current (power-generation), and *Mode-3*—restricted sag depth (power generation). The operating condition of each mode is closely related to the active-power configuration. Here, *Case-1* is used as an example to describe these LVRT modes. In this case, the active power of the PET meets

$$|P_{LA(rated)}| < P_{MD} + P_{LD} \tag{7}$$

When the grid voltage drops, the maximum active power $P_{MA(max)}$ of the MVac port can be calculated from Eqs. (2), (4), and (5), and by substituting $P_{MA(max)}$ into Eq. (6), the temporary active power of the LVac port $P_{LA(temp)}$ can be derived as

$$P_{LA(temp)} = -P_{MA(max)} - (P_{MD} + P_{LD}). \tag{8}$$

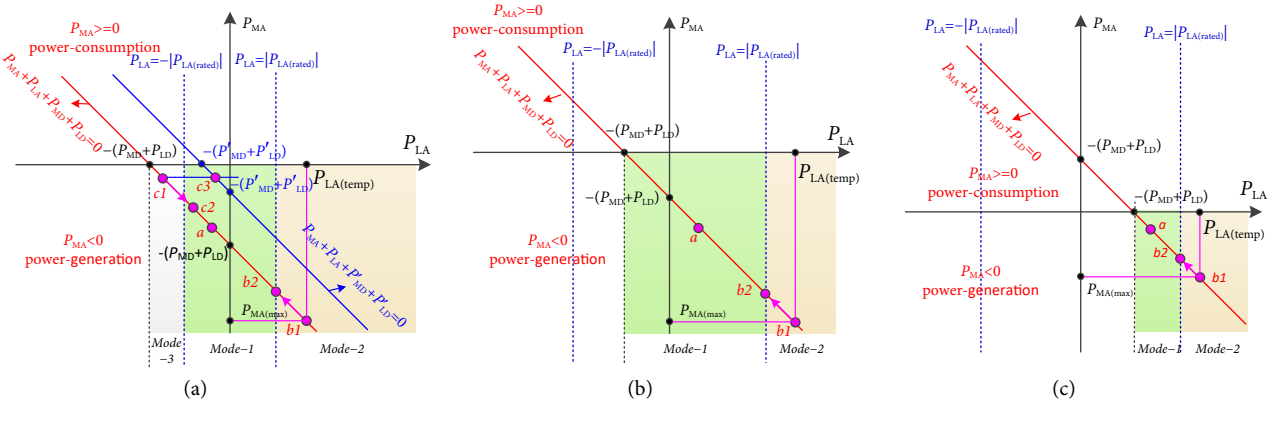

Fig. 2 LVRT mode classification of the PET under different power configurations in the power-generation state of the MVac port. (a) *Case 1*, $|P_{LA(rated)}| < P_{MD} + P_{LD}$. **(b)** *Case 2*, $|P_{LA(rated)}| \geqslant P_{MD} + P_{LD} > 0$. **(c)** *Case 3*, $|P_{LA(rated)}| > -P_{MD} - P_{LD} \geqslant 0$.

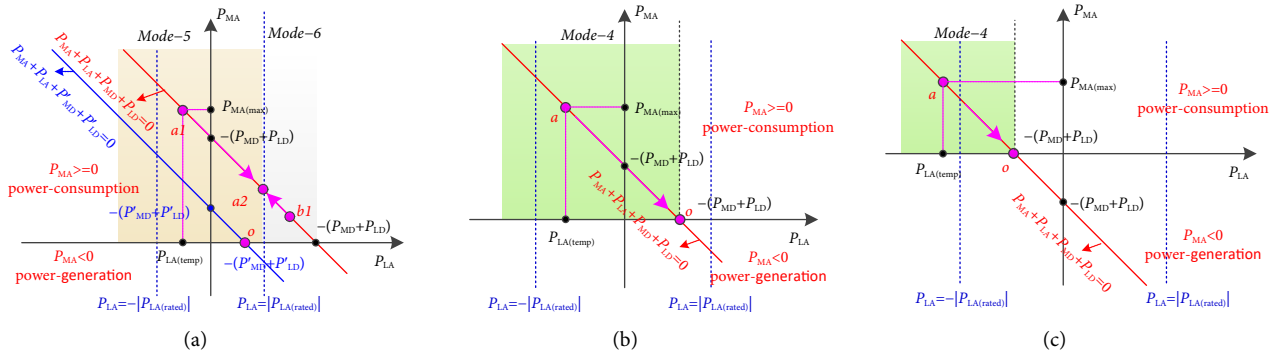

Fig. 3 LVRT mode classification of the PET under different power configurations in the power-consumption state of the MVac port. (a) *Case 4*, $|P_{LA(rated)}| \leqslant -P_{MD}-P_{LD}$. **(b)** *Case 5*, $|P_{LA(rated)}| > -P_{MD}-P_{LD} \geqslant 0$. **(c)** *Case 6*, $|P_{LA(rated)}| \geqslant P_{MD}+P_{LD} > 0$.

(1) If $|P_{LA(temp)}| < |P_{LA(rated)}|$

In this case, the operating point of PET falls on 'a' in Figure 2(a), and the PET will enter into LVRT *Mode-1*. That is, the MVac port will deliver the maximum active power $P_{MA(max)}$ to the grid. Then, the new active power of the LVac port can be set as

$$P_{LA(set)} = P_{LA(temp)}. \tag{9}$$

If the LVac-port power is adjusted according to Eq. (9), the active power among all ports will be rebalanced, and the current stress on the grid side of the MVac port can be limited.

(2) If $P_{LA(temp)} \geqslant |P_{LA(rated)}|$

In this case, the operating point of PET falls on 'b1' in Figure 2(a), and the PET will enter into LVRT *Mode-2*.

Since the active power of LVac port $P_{LA(temp)}$ exceeds the rated power $|P_{LA(rated)}|$ at 'b1', the power of PET needs to be rearranged, and the active power delivered by MVac port to the grid is limited. To ensure that active power is provided to the grid as much as possible[9], the operating point should shift from 'b1' to 'b2', as shown in Figure 2(a). In this mode, the new active power of the LVac port is set as

$$P_{LA(set)} = |P_{LA(rated)}|. \tag{10}$$

(3) If $P_{LA(temp)} \leqslant -|P_{LA(rated)}|$

In this case, the operating point of PET falls on 'c1' in Figure 2(a), and the PET will enter into LVRT *Mode-3*. Since the active power $P_{LA(temp)}$ exceeds the rated power $|P_{LA(rated)}|$ at 'c1', the operating point should move from 'c1' to 'c2'. However, at point 'c2', the active power delivered by MVac port to the grid will exceed the maximum value $|P_{MA(max)}|$ calculated according to Eq. (5). Therefore, this working condition should be avoided when the power of dc ports is constant, otherwise, the MVac port will disconnect from the grid. The voltage sag depth N_v should be restricted, and the minimum sag depth $N_{v(min)}$ meets

$$\sqrt{1-[1.5\times(0.9-N_{v(min)})]^2} = \frac{2}{3}\times\frac{P_{MD}+P_{LD}-|P_{LA(rated)}|}{U_{m(rated)}\cdot I_{m(rated)}\cdot N_{v(min)}}. \tag{11}$$

Besides, if the active power of the MVdc or LVdc ports can also be flexibly controlled during the LVRT period, then the power-balance line can be moved upward from 'the red line' to 'the blue line' in Figure 2(a), so that $|P_{LA(temp)}|$ is reduced, and the PET can operate at the point of 'c3'.

In the same way, the operating conditions of each LVRT mode under *Case-2* and *Case-3* can also be obtained, as listed in Table 1.

2.2 LVRT modes in the power-consumption state

In the power-consumption state (i.e., $P_{MA} \geqslant 0$), the MVac port should provide reactive-power support and absorb the minimum active power from the grid during the LVRT period. As shown in Figure 3, the PET's LVRT modes are divided into *Mode-4*—minimum active current, *Mode-5*—limited active current (power consumption), and *Mode-6*—restricted sag depth (power consumption). These LVRT modes under different active-power configurations are described as follows.

(1) The Case-4 of active power configuration

As shown in Figure 3(a), the active power of the PET meets

$$|P_{LA(rated)}| \leqslant -(P_{MD}+P_{LD}). \tag{12}$$

When the grid voltage drops, with the estimated grid voltage sag depth N_v, the maximum active power $P_{MA(max)}$ can be calculated from Eqs. (2), (4), and (5), and then the temporary active power of the LVac port $P_{LA(temp)}$ can also be obtained according to Eq. (8).

(a) If $P_{LA(temp)} < |P_{LA(rated)}|$

In this case, the operating point of PET falls on 'a1' in Figure 3(a). The PET will enter into LVRT *Mode-5*, and the new operating point is 'a2', where the active power absorbed by the MVac port from the grid is limited, namely, it cannot be reduced to zero to prevent the power of the LVac port from exceeding $|P_{LA(rated)}|$. In this mode, the new active power of the LVac port $|P_{LA(set)}|$ satisfies Eq. (10).

(b) If $P_{LA(temp)} \geqslant |P_{LA(rated)}|$

In this case, the operating point of PET falls on 'b1' in Figure 3(a), and the PET will enter LVRT *Mode-6*. Since the active power $P_{LA(temp)}$ exceeds the rated power $|P_{LA(rated)}|$ at 'b1', the operating point should shift from 'b1' to 'a2'. However, at point 'a2', the active power absorbed by the MVac port from the grid will exceed the maximum value $|P_{MA(max)}|$. Thus, the voltage sag depth N_v should be restricted. The minimum sag depth $N_{v(min)}$ should meet

$$\sqrt{1-[1.5\times(0.9-N_{v(min)})]^2} = -\frac{2}{3}\times\frac{P_{MD}+P_{LD}+|P_{LA(rated)}|}{U_{m(rated)}\cdot I_{m(rated)}\cdot N_{v(min)}}. \tag{13}$$

Besides, if the active power of P_{MD} or P_{LD} can also be flexibly controlled, then the power-balance line can be moved down from 'the red line' to 'the blue line' in Figure 3(a), and the PET can operate at the point of 'o'.

(2) The Case-5 and Case-6 of active power configuration

Under *Case-5* and *Case-6*, the active powers of the PET respectively meet Eqs. (14) and (15) as follows

$$|P_{LA(rated)}| > -(P_{MD}+P_{LD}) \geqslant 0 \tag{14}$$

Table 1 Operating condition of each LVRT mode in the power-generation state

Power configuration of the PET	LVRT *Mode-1*		LVRT *Mode-2*		LVRT *Mode-3*	
	Operating condition	$P_{LA(set)}$	Operating condition	$P_{LA(set)}$	Operating condition	$N_{v(min)}$
Case 1: $\lvert P_{LA(rated)}\rvert < P_{MD}+P_{LD}$	$\lvert P_{LA(temp)}\rvert < \lvert P_{LA(rated)}\rvert$		$P_{LA(temp)} \geqslant \lvert P_{LA(rated)}\rvert$		$P_{LA(temp)} \leqslant -\lvert P_{LA(rated)}\rvert$	Eq. (11)
Case 2: $\lvert P_{LA(rated)}\rvert \geqslant P_{MD}+P_{LD} > 0$	$-P_{MD}-P_{LD} \leqslant P_{LA(temp)} < \lvert P_{LA(rated)}\rvert$	$P_{LA(temp)}$	$P_{LA(temp)} \geqslant \lvert P_{LA(rated)}\rvert$	$\lvert P_{LA(rated)}\rvert$	—	—
Case 3: $\lvert P_{LA(rated)}\rvert > -P_{MD}-P_{LD} \geqslant 0$	$-P_{MD}-P_{LD} \leqslant P_{LA(temp)} < \lvert P_{LA(rated)}\rvert$		$P_{LA(temp)} \geqslant \lvert P_{LA(rated)}\rvert$		—	—

$$\lvert P_{LA(rated)}\rvert \geqslant (P_{MD}+P_{LD}) > 0. \tag{15}$$

As shown at point 'a' in Figures 3(b) and 3(c), when the grid voltage drops, the calculated $P_{MA(max)}$ will be higher than zero, and the minimum active power absorbed by the MVac port from the grid can be reduced to zero. That is, the PET will enter into LVRT *Mode-4*, and the new operating point is 'o'. In this mode, the new active power of the LVac port is

$$P_{LA(set)} = -(P_{MD}+P_{LD}). \tag{16}$$

Based on the above analysis, when the MVac port is in the power-consumption state, the operating condition of each LVRT mode can be obtained as listed in Table 2.

3 Grid-voltage sag-depth estimation

According to the analysis in Section 2, it is necessary to obtain the accurate grid-voltage sag depth as soon as possible in order to enter the correct LVRT mode, so that the power can be properly adjusted in time to avoid overcurrent protection.

As shown in Figure 4, considering the influence of harmonics, the control loop input of the phase-locked loop under the synchronous rotating frames (SRF–PLL), which is widely used nowadays, can be expressed as

$$\theta+\tilde{\theta} \approx \frac{U_{gmN}}{U_{gm}}\sin(-\omega_0 t+\sigma_N-\theta_r)+\sum_n \frac{U_{gmn}}{U_{gm}}\sin(n\omega_0 t+\sigma_n-\theta_r)+(\omega_0 t+\sigma_0) \tag{17}$$

where U_{gm}, σ_0, and ω_0 represent the amplitude, phase, and angular frequency of the fundamental positive-sequence component, respectively. θ_r is the output phase of SRF–PLL. U_{gmN} and σ_N, U_{gmn} and σ_n denote the amplitude and phase of fundamental negative-sequence, and nth harmonic component, respectively.

According to the analytical solution of step response of the control loop shown in Figure 4, the transition period t_d is inversely proportional to the coefficient k_{p1}, as expressed as

$$t_d = 8/k_{p1}. \tag{18}$$

And the overshoot PO is inversely proportional to k_{i1}/k_{p12}, which can be expressed as

$$PO = e^{\frac{1}{\sqrt{-1+4\xi}}\left(\pi-\arccos\left(1-\frac{1}{2\xi}\right)\right)} \tag{19}$$

where $\xi = k_{i1}/k_{p1}^2$.

Furthermore, as shown in Figure 5, the smaller the k_{p1}, the bigger the attenuation gain, but the transition period t_d will increase. For the 5th and 7th harmonics, the attenuation gains are still less than 20 dB when t_d is 40 ms. Therefore, it is necessary to add multiple notch filters (NF)[18] in the control loop to filter out high-order harmonics, namely the NF–SRF–N_v algorithm. However, it is unable to achieve a rapid estimation of voltage sag depth, according to the verification with experiments in Section 6.

As shown in Figure 6, the estimation scheme of NF–LPF–N_v is proposed in this paper, where LPF and NF represent the low-pass filter and the notch filter to attenuate the high-order and second-order harmonics, respectively. Their discrete transfer functions[19] can be expressed as

$$F_{LPF}(z) = \frac{\omega_c}{s+\omega_c}\Big|_{s=\frac{2}{T_s}\frac{z-1}{z+1}} \tag{20}$$

$$F_{N2}(z) = \frac{(1+a_2)-2a_1 z^{-1}+(1+a_2)z^{-2}}{2(1-a_1 z^{-1}+a_2 z^{-2})} \tag{21}$$

$$\begin{cases} a_1 = \dfrac{2\cos(2\omega_0 T_s)}{1+\sqrt{10^{\chi/10}-1}\cdot\tan(\Omega T_s/2)} \\ a_2 = \dfrac{1-\sqrt{10^{\chi/10}-1}\cdot\tan(\Omega T_s/2)}{1+\sqrt{10^{\chi/10}-1}\cdot\tan(\Omega T_s/2)} \end{cases} \tag{22}$$

where ω_c is the LPF cutoff frequency, T_s is the control period, χ represents the attenuation gain of NF at $\omega = 2\omega_0 \pm \Omega/2$, and Ω is its bandwidth.

According to the Bode plot of $F_{LPF}(z)\cdot F_{N2}(z)$, the attenuation gain also conflicts with the transient respond speed. When the compromised design result is that ω_c = 377 rad/s, Ω = 80 Hz, χ = 3 dB, the transition period of NF–LPF–N_v is about 10 ms. Its performances are also tested with experiments in Section 6.

4 Active-power regulation path optimization during the LVRT transition

According to the experimental results in Section 6, a lag of about 10 ms exists in the voltage sag-depth estimation, meaning that the estimated N_v cannot track the actual voltage sag depth N_{v_o} in time. Here, this lag is defined as the transition period of LVRT, that is, the interval from the voltage sudden change to the accurate detection of the voltage sag depth. Correspondingly, the LVRT transition process can be divided into two types, namely, voltage sag and

Table 2 Operating condition of each LVRT mode in the power-consumption state

Power configuration of the PET	LVRT *Mode-4*		LVRT *Mode-5*		LVRT *Mode-6*	
	Operating condition	$P_{LA(set)}$	Operating condition	$P_{LA(set)}$	Operating condition	$N_{v(min)}$
Case 4: $\lvert P_{LA(rated)}\rvert \leqslant -P_{MD}-P_{LD}$	—	—	$P_{LA(temp)} < \lvert P_{LA(rated)}\rvert$	$\lvert P_{LA(rated)}\rvert$	$P_{LA(temp)} \geqslant \lvert P_{LA(rated)}\rvert$	Eq. (13)
Case 5: $\lvert P_{LA(rated)}\rvert > -P_{MD}-P_{LD} \geqslant 0$	$P_{LA(temp)} < -P_{MD}-P_{LD}$	$-P_{MD}-P_{LD}$	—	—	—	—
Case 6: $\lvert P_{LA(rated)}\rvert \geqslant P_{MD}+P_{LD} > 0$	$P_{LA(temp)} < -P_{MD}-P_{LD}$		—	—	—	—

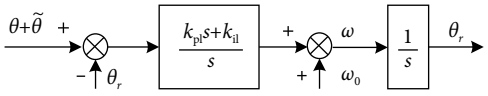

Fig. 4 Control loop of the SRF–PLL.

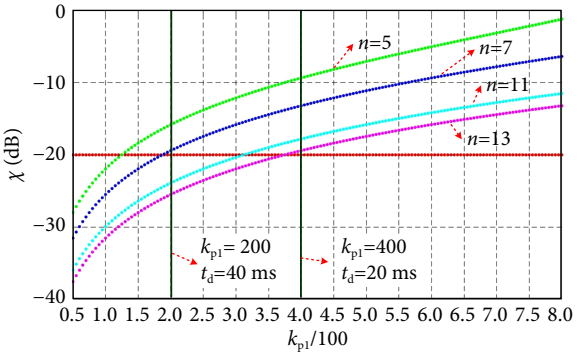

Fig. 5 Relationship between the attenuation gain χ for high-order harmonics and k_{p1} when *PO* is fixed at 0.2.

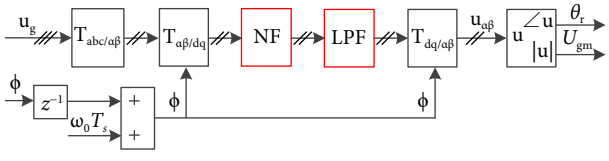

Fig. 6 The grid-voltage sag-depth estimation scheme NF–LPF–N_v.

voltage recovery. During the LVRT transition, there are multiple paths for regulating the active-power flow of the MVac port, and it should be decided to prevent overcurrent protection.

From Eqs. (2), (4), and (5), the maximum active power of the MVac port can be represented as

$$\left|P_{\mathrm{MA(max)}}\right| = f(N_{\mathrm{v}}) = \begin{cases} 0 & 0.2 \leqslant N_{\mathrm{v}} \leqslant 0.234 \\ \dfrac{3U_{\mathrm{gm(rated)}}\ I_{\mathrm{m(rated)}}\ N_{\mathrm{v}}\sqrt{1-[1.5\times(0.9-N_{\mathrm{v}})]^2}}{2} & 0.9 \geqslant N_{\mathrm{v}} > 0.234 \end{cases} \tag{23}$$

where N_v represents the estimated grid-voltage sag depth.

From Eq. (23), the maximum active-power curve of the MVac port '$|P_{\mathrm{MA(max)}}|$—N_v' can be obtained, as shown in Figures 7 and 8, where $|P_{\mathrm{MAfb}}|$ represents the pre-fault active power. Furthermore, if the actual grid-voltage sag depth is N_{v_o}, the maximum active power that the MVac port can actually exchange with the grid can be expressed as

$$\left|P_{\mathrm{MA\_O}}\right| = f(N_{\mathrm{v\_o}}). \tag{24}$$

According to the active-power configurations in Figures 2 and 3 and the rated power of the LVac port $|P_{\mathrm{LA(rated)}}|$, the limited active power of the MVac port can be expressed as

$$P_{\mathrm{MA\_O^*}} = -(P_{\mathrm{MD}} + P_{\mathrm{LD}} + |P_{\mathrm{LA(rated)}}|). \tag{25}$$

4.1 LVRT transition process in the power-generation state

Figure 7 shows the active-power regulation paths during the LVRT transition period in the power-generation state.

(1) If $|P_{\mathrm{MAfb}}| \leqslant |P_{\mathrm{MA\_O}}| \leqslant |P_{\mathrm{MA\_O}^*}|$

As shown in Figure 7(a), once the grid voltage drops, the estimated sag depth N_v will gradually change from 0.9 to the actual value N_{v_o}. However, the active power of the MVac port is controlled directly according to N_v instead of N_{v_o} as described in Section 2, and its regulation path during the LVRT transition period will be 'A→B→O*→O'. In this process, the active power delivered to the grid will exceed $|P_{\mathrm{MA\_O}}|$, which can easily cause overcurrent protection. To avoid this defect, the active-power regulation path is optimized and changed to 'A→D→O'. In the section of 'A→D', the active power remains unchanged. The PET will enter into *Mode-1* in section 'D→O' and finally reach the new equilibrium point 'O'.

In the process of voltage recovery, the power regulation path is 'O→O*→B→A'. In the section of 'O→O*', the PET works in the LVRT *Mode-1*, and it will enter into the LVRT *Mode-2* in section 'O*→B'. When the N_v is restored to above 0.9, the active power of MVac port returns to $|P_{\mathrm{MAfb}}|$.

(2) If $|P_{\mathrm{MA\_O}}| > |P_{\mathrm{MA\_O}^*}|$

As shown in Figure 7(b), the active power of the MVac port is given according to the path 'A→D→O*' in the process of voltage sag. The new equilibrium point is 'O*', where the PET works in the LVRT *Mode-2*. During the voltage recovery process, the active-power regulation path is 'O*→B→A'.

(3) If $|P_{\mathrm{MA\_O}}| < |P_{\mathrm{MAfb}}|$

As shown in Figure 7(c), during the voltage sag transition, the active-power regulation path of the MVac port is set to 'A→D→O'. In the process of voltage recovery, it becomes 'O→O*→B→A'.

4.2 LVRT transition process in the power-consumption state

If $P_{\mathrm{MA\_O^*}} \geqslant 0$, as shown in Figure 8(a), the active-power regulation path is 'A→B→O*' during the transition of the voltage sag. The PET enters LVRT *Mode-5* immediately when it is detected that N_v is less than 0.9. After that, the active power is maintained at $P_{\mathrm{MA\_O^*}}$. In the process of voltage recovery, the active-power regulation path is 'O*→B→A'.

As shown in Figure 8(b), which indicates that $P_{\mathrm{MA\_O^*}} < 0$, the active power regulation paths are 'A→B→D' and 'D→B→A' during the grid-voltage sag and recovery process, respectively. In section 'B—D', the PET works in the LVRT *Mode-4*.

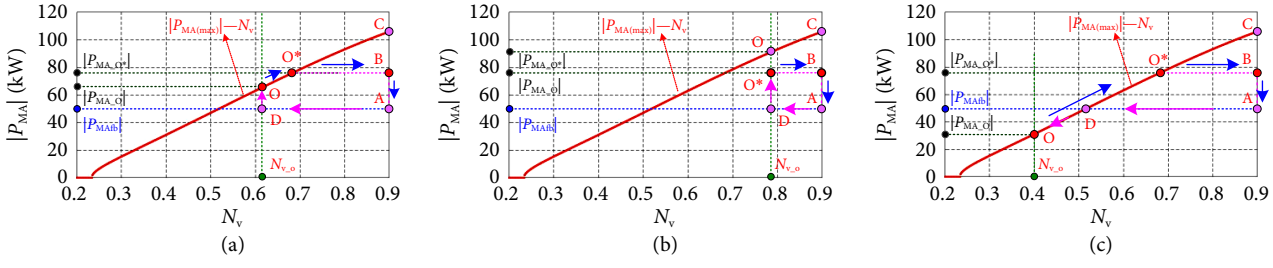

Fig. 7 Active-power regulation path during LVRT transition in the power-generation state. (a) $|P_{\mathrm{MAfb}}| \leqslant |P_{\mathrm{MA\_O}}| \leqslant |P_{\mathrm{MA\_O}^*}|$. **(b)** $|P_{\mathrm{MA\_O}}| > |P_{\mathrm{MA\_O}^*}|$. **(c)** $|P_{\mathrm{MA\_O}}| < |P_{\mathrm{MAfb}}|$.

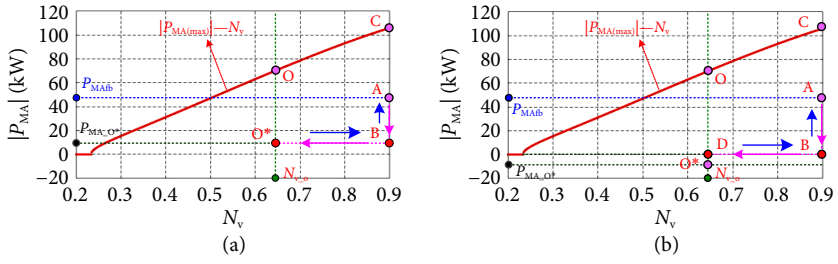

Fig. 8 Active-power regulation path during LVRT transition in the power-consumption state. (a) $P_{MA\_O}^* \geqslant 0$. **(b)** $P_{MA\_O}^* < 0$.

5 Control strategy and parameter design

In this section, the control strategies and parameters of the HFB–PET are designed. Figure 9 shows the block diagram of the control system.

5.1 Grid-side converter of the MVac port

(1) Control strategies

A dual-loop control strategy[20] is adopted for the grid-side converter of the MVac port, and the inner current loop is shown in Figure 9(b), where $\boldsymbol{u}_c$ is the feedforward voltage. Since the grid-side filter inductance is generally small, $\boldsymbol{u}_c$ should be consistent with the grid voltage to avoid instantaneous overcurrent when the grid voltage changes suddenly. The grid voltage $\boldsymbol{u}_g$ measured in the abc frame is directly taken as the feedforward without additional calculation. Simultaneously, the leading correction factor $G_{com}(s)$ is also used to compensate for the control delay.

$$G_{com}(s) = \left(G_d(s) \cdot G_t(s)\right)^{-1} = e^{(T_{sd}+0.5T_{hd})s} \tag{26}$$

where T_{sd} is the sampling delay, and T_{hd} is the hold delay. It can be realized by introducing a compensation angle θ_c.

$$\theta_c = \omega_0 \cdot (T_{sd} + 0.5T_{hd}) = \omega_0 \cdot T_d. \tag{27}$$

In the grid-side converter, only the d-axis current I_d impacts the dc-link voltage, and the following relationship is satisfied

$$\begin{cases} i_{co} \cdot \bar{U}_{MA} \cdot 3N_{MA} = -(P_{MD} + P_{LD} + P_{LA}) \\ i_{ci} \cdot \bar{U}_{MA} \cdot 3N_{MA} = P_{MA} = 3(I_d U_{gm})/2 \\ i_c = i_{ci} - i_{co} = C_{dc}\left(d\bar{U}_{MA}/dt\right) \end{cases} \tag{28}$$

where C_{dc} is the dc-link capacitance, $\bar{U}_{MA}$ is the average dc-link voltage, and i_{ci}, i_c, and i_{co} are the dc-side currents.

From Eq. (28), the outer loop of the dc-link voltage control with power feedforward is shown in Figure 9(c), where $G_{iloop}(s)$ is the transfer function of the d-axis current, and $|I_{p(max)}|$ represents the threshold of the active current, which is crucial to prevent overcurrent protection and is calculated from Figure 9(a) and Eq. (4).

(2) Control parameters design

Taking the d-axis current loop in Figure 9(b) as an example, the transfer function can be expressed as

$$G_{iopen}(s) = \frac{K_{Ii} + K_{Pi}s}{s} \cdot \frac{1}{R_g + L_g s} \cdot \frac{1}{1 + T_d s}. \tag{29}$$

To simplify the order of the model in Eq. (29), the PI controller is designed with the method of zero-pole cancellation. It can be seen from the power stage parameters in Table 3 that

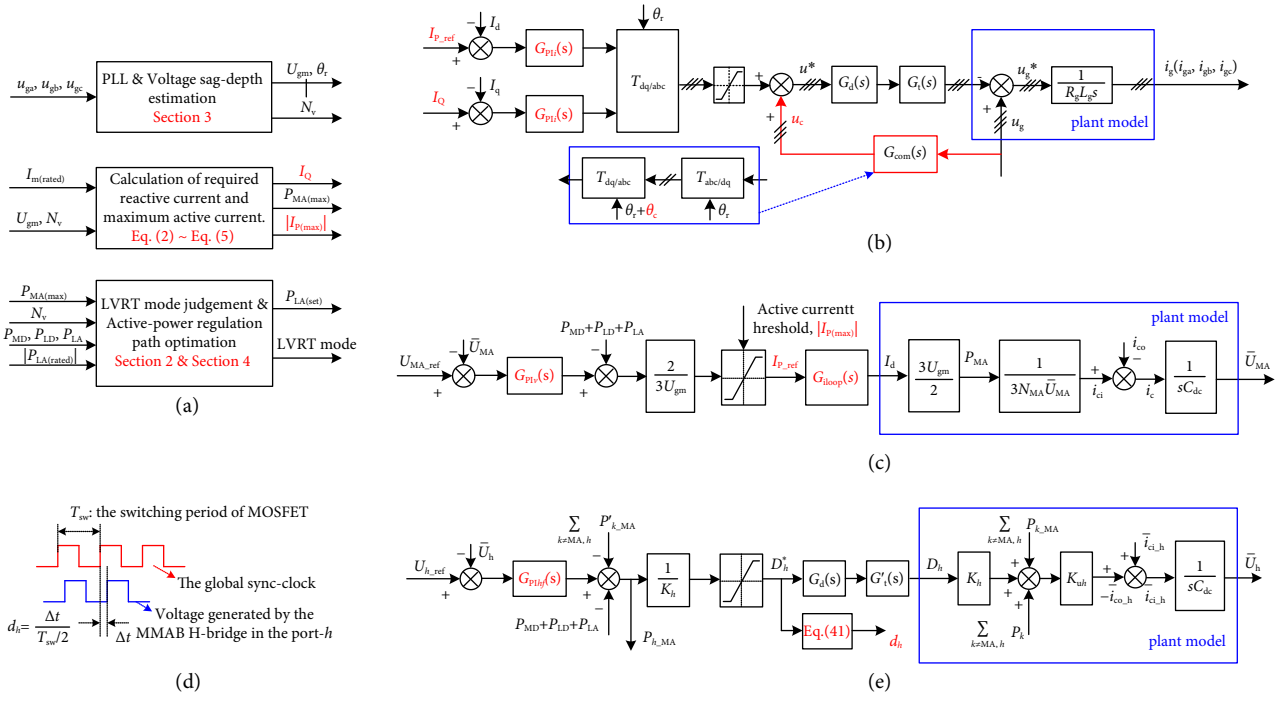

Fig. 9 Block diagram of system control strategies. (a) LVRT strategies. **(b)** and **(c)**, inner current loop and outer voltage loop of the grid-connected converter of MVac port, respectively. **(d)** Definition of the phase-shift ratio of port-h. **(e)** The control loop of MMAB, h = MD, LD, or LA.

Table 3 Power stage parameters of the four-port PET

Parameter	Value
Rated phase-to-ground voltage of MVac port, $U_{gm(rated)}$	980 V
Rated phase-to-ground voltage of LVac port, $U_{sm(rated)}$	311 V
DC-link voltage of each MMAB H-bridge, U_{h_ref}	700 V
Number of power cells, N_{MA}, N_{MD}, N_{LD}, N_{LA}	3, 2, 1, 1
Power-cell dc-link capacitance, C_{dc}	3 mF
Turns ratio of each HFT	1: 1
HFT equivalent leakage inductance, $L_{MA}/L_{MD}/L_{LD}/L_{LA}$	12.8 μH
Limited current amplitude of the MVac port, $I_{m(rated)}$	73.3 A
CHB filter inductor, L_g, R_g	5.4 mH, 54 mΩ
Grid-connected inverter filter inductor, L_s, R_s	600 μH, 6 mΩ
Control frequency, $f_{control}$	10 kHz
MMAB switching frequency, f_{sw}	20 kHz
Equivalent switching frequency of CHB, f_{CHB}	20 kHz
Switching frequency of grid-connected inverter, f_{sw_LA}	10 kHz

$$R_g / L_g \ll 1 / T_d. \tag{30}$$

Therefore, the zero point of the PI controller can be designed to cancel the pole of the plant model rather than that of the delayed item to improve the response speed of the current loop. In this case, the PI controller should satisfy

$$K_{Ii} = K_{Pi} \cdot R_g / L_g. \tag{31}$$

With the relationship of Eq. (31), the current loop appears as a second-order system. In order for under-damping characteristics, the proportional coefficient should meet

$$K_{Pi} > L_g / (4T_d). \tag{32}$$

And the transition period t_d is mainly related to the delay time, namely

$$t_d \approx 8T_d. \tag{33}$$

From Eqs. (29) and (31), the root locus diagram of the current loop can be drawn in Figure 10. In the under-damping area, as K_{Pi} increases, the system damping ratio decreases and the overshoot increases. Here, the damping ratio is chosen to be 0.707, thus the coefficient K_{Pi} can be determined.

According to Figure 9(c), the transfer function of the voltage loop can be expressed as

$$G_{vopen}(s) = \left(K_{Pv} + \frac{K_{Iv}}{s}\right) G_{iloop}(s) \cdot \left(\frac{1}{3N_{MA} \cdot U_{MA\_ref}} \cdot \frac{1}{sC_{dc}}\right) \tag{34}$$

where $G_{iloop}(s)$ is the closed-loop transfer function of the d-axis current, and it can be derived from Eqs. (29) and (31) as

$$G_{iloop}(s) = K_{Pi} / (T_d L_g s^2 + L_g s + K_{Pi}). \tag{35}$$

Since the response of the current loop is much faster than that of the voltage loop, it can be firstly considered as

$$G_{iloop}(s) = 1. \tag{36}$$

Then, the voltage loop is simplified as a second-order system. According to the analytical solution of its step response, if the damping ratio is less than 1, the control parameters should satisfy

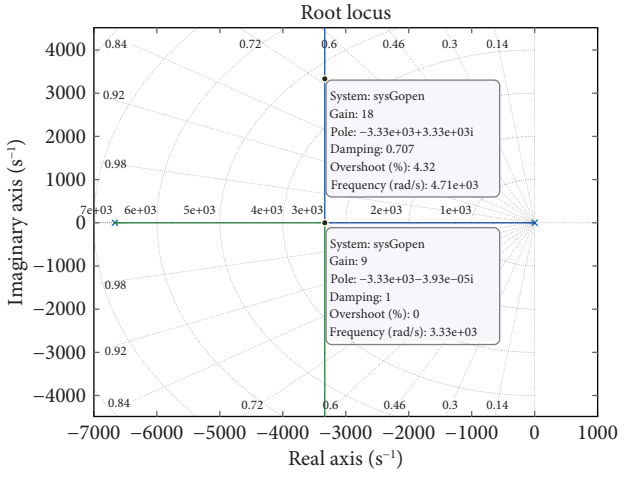

Fig. 10 Root locus diagram of the current loop.

$$K_{Pv} = \frac{24 \cdot N_{MA} U_{MA\_ref} C_{dc}}{t_{dv}} = \frac{24 \cdot N_{MA} U_{MA\_ref} C_{dc}}{N_{tdv} \cdot 10^{-3}} = \frac{k_{pref}}{N_{tdv}} \tag{37}$$

$$K_{Iv} = m \cdot K_{Pv}^2 / (12 N_{MA} U_{MA\_ref} C_{dc}), \quad m > 1 \tag{38}$$

where t_{dv} and N_{tdv} both represent the transition time of the voltage loop. According to Eq. (33), the response time of the current loop is about 1.2 ms. Therefore,

$$K_{Pv} < k_{pref} / 1.2. \tag{39}$$

From Eqs. (38) and (39), the selection ranges of K_{Pv} and K_{Iv} can be preliminarily determined.

Based on this range and the parameters in Table 3, the zero-pole distribution of the voltage loop expressed in Eqs. (34) and (35) can be obtained in Figure 11, where m is 2.3.

From Figure 11, the control laws can be concluded as follows.

(a) If $N_{tdv} > 5.0$, the system damping ratio is about 0.7, otherwise, it is significantly reduced.

(b) As N_{tdv} increases, two poles will approach the imaginary axis, and the system response will slow down.

In addition, the damping ratio of the system will decrease significantly and its dynamic performance will become worse when m deviates from 2.3. Therefore, the PI parameters of the voltage loop can be taken as $K_{Pv} = k_{pref}/5.0$, $m = 2.3$.

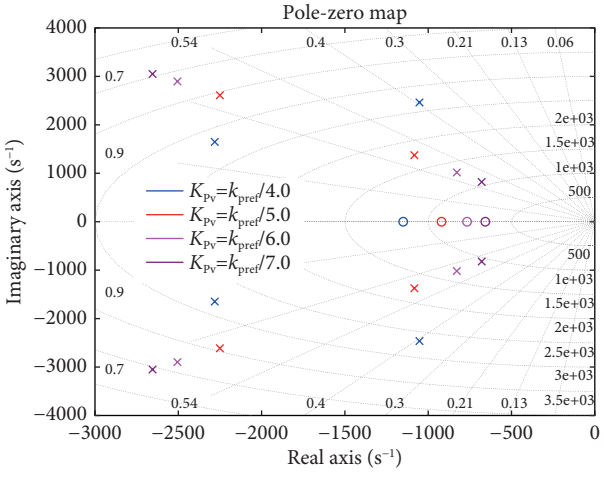

Fig. 11 The zero-pole distribution of the voltage loop, where *m* is 2.3.

5.2 MMAB converter

(1) Control strategies

As the core of the HFB–PET in Figure 1, the modular multi-active bridge (MMAB) converter is controlled with the method of the single-phase shift (SPS)[20]. A global sync-clock signal is provided in the control system, based on which the phase-shift ratio of the MMAB H-bridge can be defined as shown in Figure 9(d). As the phase-shift ratios of all MMAB H-bridges in each port are the same, they can be expressed by a uniform quantity, that is, d_h denotes the phase-shift ratio of the port h. By adjusting d_h, the power flow between any two ports can be controlled.

For the MVac port, the output voltage of the MMAB H-bridge is in phase with the sync-clock, namely, $d_{MA} = 0$.

For other ports, the power cross decoupling strategy is used to control the dc-side voltage, and the control diagram of the port h is shown in Figure 9(e), where U_{h_ref} is the reference voltage, and K_{uh}, K_h, and D_h are described as

$$K_{uh} = \frac{1}{N_h \cdot U_{h\_ref}},\ K_h = \frac{\bar{U}_{MA}\bar{U}_h}{2f_{sw} \cdot L_{MA}L_h \cdot \left(\frac{1}{L_{MA}} + \frac{1}{L_{MD}} + \frac{1}{L_{LD}} + \frac{1}{L_{LA}}\right)} \quad (40)$$

$$D_h = d_h(1 - |d_h|) \quad (41)$$

in which $\bar{U}_h$ is the average dc-link voltage, and L_{MA}, L_{MD}, L_{LD}, and L_{LA} represent the equivalent inductance of the MVac, MVdc, LVdc, and LVac ports, respectively.

(2) Control parameters design

According to Figure 9(e), the transfer function of the MMAB control loop can be expressed as

$$G_{MMAB}(s) = \left(K_{Phf} + \frac{K_{Ihf}}{s}\right) \cdot \frac{1}{1 + (T_{sd} + 0.5T'_{hd})s} \cdot \left(\frac{1}{N_h U_{h\_ref}} \frac{1}{sC_{dc}}\right) \quad (42)$$

where T_{sd} and T'_{hd} are the sampling and hold delay, respectively.

By comparing Eqs. (34) and (42), it can be found that the form of $G_{MMAB}(s)$ is similar to that of $G_{vopen}(s)$. Therefore, the same method can be used for the MMAB controller design. Finally, K_{Phf} and K_{Ihf} are obtained as listed in Table 4, and the transition period of the MMAB control loop is about 1.6 ms.

Table 4 Control parameters of the four-port PET

Parameter	Value
Voltage controller of MVac port, K_{Pv},K_{Iv}	30240.0, 2.7821×10^7
Current controller of MVac port, K_{Pi}, K_{Ii}	−18.0, −180.0
Voltage controller of MMAB, K_{Phf}, K_{Ihf}	6720.0, 8.064×10^6
Current controller of LVac port, K_{Pi}, K_{Ii}	−2.0, −20.0

5.3 Grid-side converter of the LVac port

The LVac port always runs in the P/Q mode, and the control diagram of the grid-side converter is the same as that in Figure 9(b). The active-current reference is expressed as

$$I_{P\_ref\_LA} = 2P_{LA(set)} / (3U_{sm}) \quad (43)$$

where $P_{LA(set)}$ is determined by the LVRT strategies shown in Figure 9(a), and U_{sm} is the amplitude of the LV grid voltage.

6 Experimental results

6.1 Experimental platform and key parameters

In order to prove the feasibility of the proposed control algorithm, the PET system based on the hardware-in-the-loop platform is implemented as shown in Figure 12. The power stage model is performed on the NI PXIe-7868R boards of the real-time simulation system. The system controller is designed with the 'DSP+FPGA' platform. The analog/digital signals interaction between the real-time simulation system and the controller is realized by the I/O boards, and the signals on I/O boards can be sent to the scope order for display. The related parameters are shown in Tables 3 and 4.

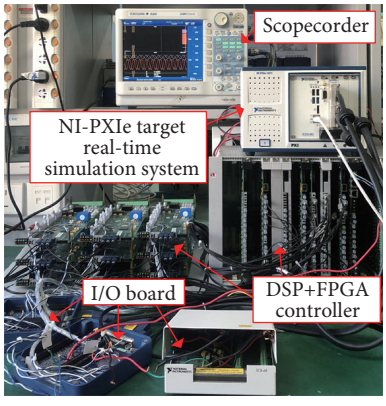

Fig. 12 Hardware-in-the-loop experimental platform.

6.2 Performance of the proposed grid-voltage sag-depth estimation

In this section, experimental tests are performed to verify the effectiveness of the algorithm NF–LPF–N_v designed in Section 3. Meanwhile, the other two estimation methods including NF–SRF–N_v and FAE–N_v[15] are also compared with it. The parameters of NF–SRF–N_v which are illustrated in Figure 4 are set as k_{pl} = 267.0 and k_{il} = 35645.0, and some NFs are added to filter out high-order harmonics. The parameter of the FAE–N_v is chosen as γ = 0.045, and the nominal frequency is 50 Hz.

As shown in Figure 13, when the voltage sag depth is 0.5, the proposed algorithm NF–LPF–N_v exhibits faster dynamics with a settling time of about 10 ms, while the other two estimation methods are both about 15 ms. Moreover, obvious fluctuations exist in the estimation process of the NF–SRF–N_v method, which will be detrimental to the LVRT mode judgment.

As shown in Figure 14, when the voltage sag depth is 0.5 and the THDs of 1th, 5th, 7th, and 11th components are all 10%, the NF–LPF–N_v can estimate the distorted grid voltage faster. Furthermore, the harmonic attenuation capability of FAE–N_v is much weaker.

Figure 15(a) shows the experimental results when the voltage sag depth is 0.5 while the frequency jumps from 50 to 51 Hz. When the phase is suddenly increased by 45°, the comparison results are shown in Figure 15(b). The results indicate that the proposed algorithm NF–LPF–N_v has faster dynamics and is more robust to frequency and phase jumps.

In conclusion, the proposed algorithm NF–LPF–N_v is a promising solution for LVRT because it is much faster than the PLL–based method[16], while the estimation process is smooth and it has stronger harmonic attenuation capability.

6.3 LVRT operation results in the power-generation state

As listed in Table 3, the input-current amplitude of the MVac port is limited to 73.3 A. During the LVRT period, this threshold cannot be exceeded.

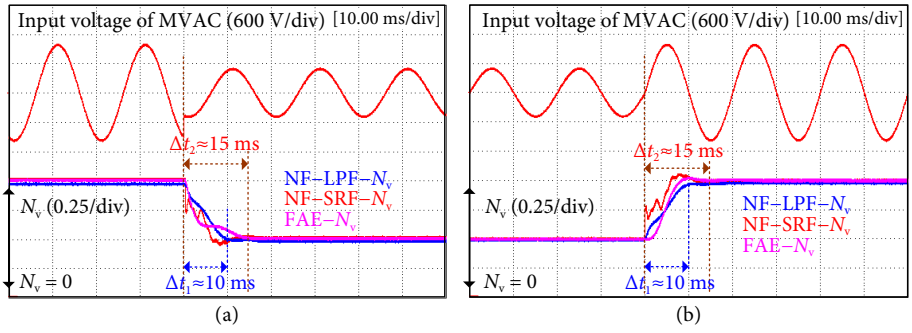

Fig. 13 Experimental results with a voltage sag-depth of 0.5. (a) Sag transition. **(b)** Recovery transition.

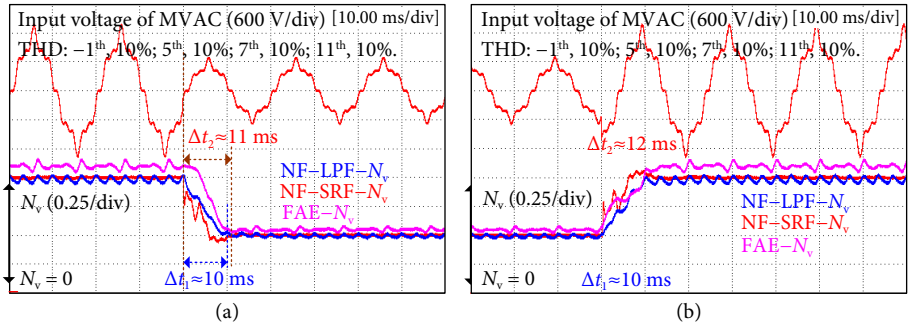

Fig. 14 Experimental results when the voltage sag depth is 0.5, and the THDs of 1th, 5th, 7th, and 11th components are all 10%. (a) Sag transition. **(b)** Recovery transition.

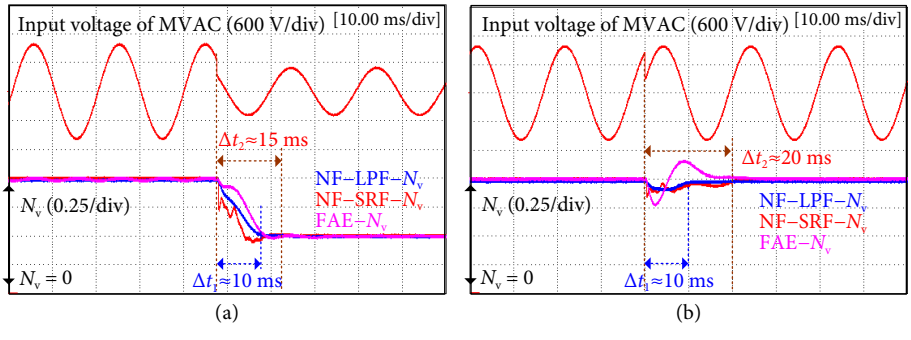

Fig. 15 Experimental results. (a) Voltage sag of 0.5 p.u. and frequency jump of 1 Hz. **(b)** Phase sudden change of 45°.

When the MVac port is in the power-generation state, there are three power configuration cases, namely, *Case-1*, *Case-2*, and *Case-3*, as shown in Figure 2. Each case corresponds to multiple LVRT modes. The pre-fault settings for verifying the LVRT performance in different cases are as follows.

(a) LVRT *Mode-1* in *Case-1*: $P_{MD} = -20$ KW, $P_{LD} = 100$ KW, $P_{LA} = 0$, $P_{MAfb} = -80$ KW, $Q_{MA} = 0$, $|P_{LA(rated)}| = 70$ KW.

(b) LVRT *Mode-2* in *Case-1*: $P_{MD} = -20$ KW, $P_{LD} = 80$ KW, $P_{LA} = 0$, $P_{MAfb} = -60$ KW, $Q_{MA} = 0$, $|P_{LA(rated)}| = 20$ KW.

(c) LVRT *Mode-1* in *Case-2*: $P_{MD} = -20$ KW, $P_{LD} = 60$ KW, $P_{LA} = 0$, $P_{MAfb} = -40$ KW, $Q_{MA} = 0$, $|P_{LA(rated)}| = 70$ KW.

(d) LVRT *Mode-2* in *Case-2*: $P_{MD} = -20$ KW, $P_{LD} = 50$ KW, $P_{LA} = 0$, $P_{MAfb} = -30$ KW, $Q_{MA} = 0$, $|P_{LA(rated)}| = 40$ KW.

(e) LVRT *Mode-1* in *Case-3*: $P_{MD} = -20$ KW, $P_{LD} = -20$ KW, $P_{LA} = 100$ KW, $P_{MAfb} = -60$ KW, $Q_{MA} = 0$, $|P_{LA(rated)}| = 120$ KW.

(f) LVRT *Mode-2* in *Case-3*: $P_{MD} = -20$ KW, $P_{LD} = -20$ KW, $P_{LA} = 100$ KW, $P_{MAfb} = -60$ KW, $Q_{MA} = 0$, $|P_{LA(rated)}| = 120$ KW.

Experimental results of LVRT *Mode-1* in *Case-1* are presented in Figure 16. Figures 16(a) and 16(c) show the transitions of voltage sag and voltage recovery, respectively. The power and current command responses of the PET are shown in Figures 16(b) and 16(d). When the grid voltage is symmetrically dropped from 0.96 to 0.35 p.u. or restored from 0.35 to 0.96 p.u., the actual grid-voltage sag depth is detected in 10 ms without fluctuations.

As shown in Figure 16(b), in the LVRT transition (i.e., t_1–t_3), the reactive current $I_{Q(set)}$ is set according to Eqs. (2) and (3), and the active-current threshold $I_{P(limit)}$ is consistent with $I_{P(max)}$ expressed in Eq. (4). After t_3, the estimated grid-voltage sag depth N_v is stable (i.e., $N_v = N_{v\_o} = 0.35$) and $I_{P(limit)}$ reaches −41.5 A, while $I_{Q(set)} = 60.5$ A and $Q_{MA(set)} = -31.1$ kVar. According to Eqs. (5) and (8), the maximum active power $P_{MA(max)}$ and the temporary active power $P_{LA(temp)}$ can also be determined when $N_v = 0.35$, that is, $P_{MA(max)} = -21.3$ kW and $P_{LA(temp)} = -58.7$ kW. Since $|P_{LA(temp)}| < |P_{LA(rated)}|$, the PET enters into the LVRT *Mode-1*, the active power delivered to the grid is equal to $P_{MA(max)}$, and the new active power $P_{LA(set)}$ is equal to $P_{LA(temp)}$. Furthermore, in this process, the active power of the PET is regulated according to the optimized path shown in Figure 7(c), and $P_{LA(set)}$ remains zero during the period of t_1–t_2.

As shown in Figure 16(d), in the LVRT transition of the voltage

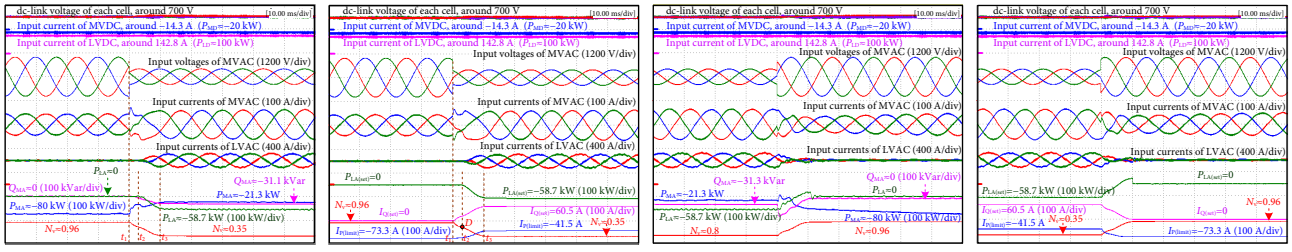

Fig. 16 Experimental results of LVRT *Mode-1* in *Case-1* of active-power configuration. **(a)** Real-time power curve in the voltage sag process. **(b)** Power command curve in the voltage sag process. **(c)** Real-time power curve in the voltage recovery process. **(d)** Power command curve in the voltage recovery process.

recovery, the reactive current $I_{Q(set)}$ and the active-current threshold $I_{P(limit)}$ are set according to Eqs. (2), (3), and (4) too. The active power regulation path meets that in Figure 7(c).

Figure 17 shows experimental results of LVRT *Mode-2* in *Case-1* of power configuration under a voltage sag depth of 0.8. In this case, $P_{MA(max)} = -85.2$ kW, $P_{LA(temp)} = 25.2$ kW. Since $|P_{LA(temp)}| > |P_{LA(rated)}|$, the PET enters into the LVRT *Mode-2*, the active power delivered to the grid is limited and less than $P_{MA(max)}$, and the setting power $P_{LA(set)}$ is equal to $|P_{LA(rated)}|$. The active-power regulation path meets that in Figure 7(b).

Figure 18 shows experimental results of LVRT *Mode-1* in *Case-2* of power configuration under a voltage sag depth of 0.8. The active power of the PET is regulated according to the path shown in Figure 7(a).

Figure 19 shows experimental results of LVRT *Mode-2* in *Case-2* of power configuration under a voltage sag depth of 0.8. The active power of the PET is regulated according to the path shown in Figure 7(b).

Figures 20 and 21 show experimental results of LVRT *Mode-1* and *Mode-2* in *Case-3* of power configuration, while the voltage sag depths are 0.3 and 0.8, respectively. And their active-power regulation paths meet that in Figures 7(c) and 7(b), respectively.

As shown in Figures 16(c) and 20(c) , when the grid-voltage recovers, the reference of the reactive current will lag due to the

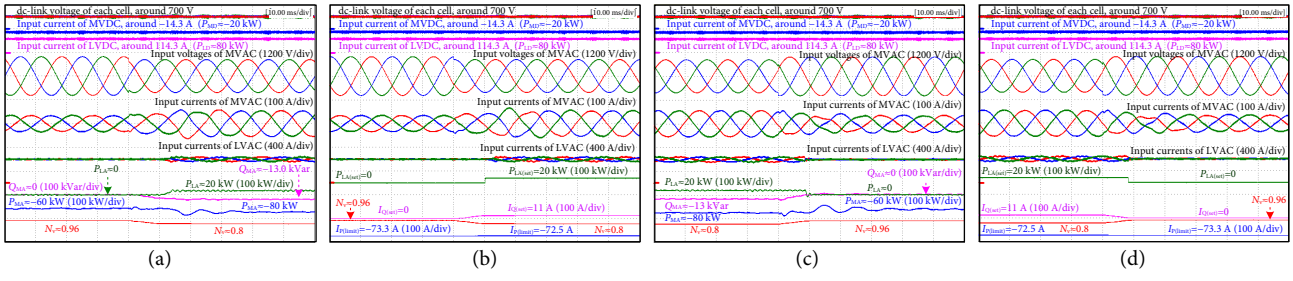

Fig. 17 Experimental results of LVRT *Mode-2* in *Case-1* of active-power configuration. **(a)** Real-time power curve in the voltage sag process. **(b)** Power command curve in the voltage sag process. **(c)** Real-time power curve in the voltage recovery process. **(d)** Power command curve in the voltage recovery process.

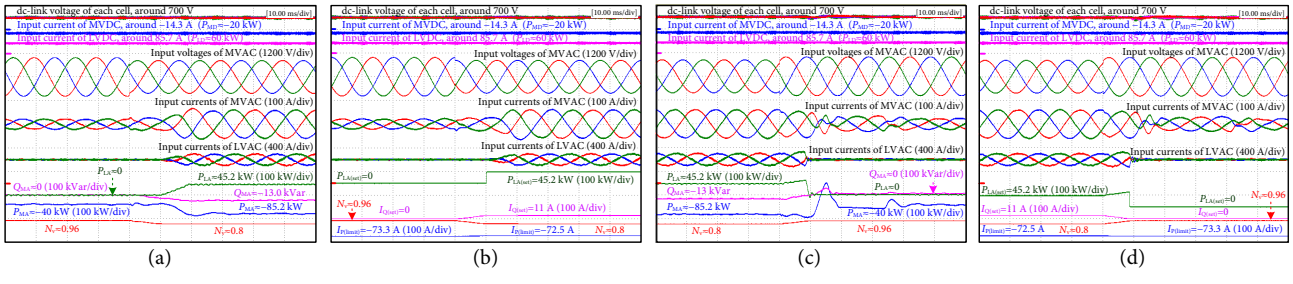

Fig. 18 Experimental results of LVRT *Mode-1* in *Case-2* of active-power configuration. **(a)** Real-time power curve in the voltage sag process. **(b)** Power command curve in the voltage sag process. **(c)** Real-time power curve in the voltage recovery process. **(d)** Power command curve in the voltage recovery process.

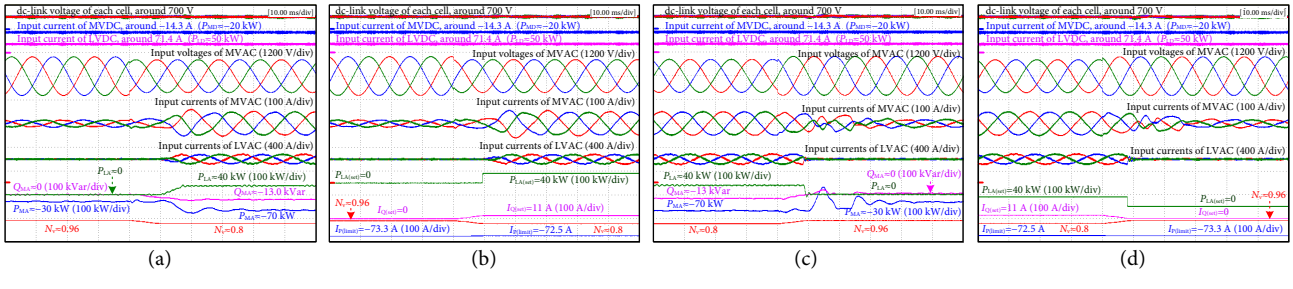

Fig. 19 Experimental results of LVRT *Mode-2* in *Case-2* of active-power configuration. **(a)** Real-time power curve in the voltage sag process. **(b)** Power command curve in the voltage sag process. **(c)** Real-time power curve in the voltage recovery process. **(d)** Power command curve in the voltage recovery process.

delay in the detection of the sag depth, which is likely to cause a sudden increase in the reactive power. In addition, the active power shown in Figures 18(c) and 19(c) has an overshoot because of the deviation of the PI coefficients.

From Figures 16(a)–21(a), with the proposed strategy, the MVac-port can provide reactive-power support within 10ms and deliver active power to the grid within 20 ms when the grid-voltage drops. The results shown in Figures 16(c)–21(c) indicate that the active power is restored to the pre-fault value within 40 ms, and the reactive power is restored within 10 ms when the grid-voltage fault disappears. These response times are all far less than the standards specified by China's GB/T19964-2012 guidelines[2].

6.4 LVRT operation results in the power-consumption state

When the MVac-port is in the power-consumption state, there are also three power configuration cases, namely, *Case*-4, *Case*-5, and *Case*-6, as shown in Figure 3. The pre-fault settings for verifying the LVRT performance in different cases are as follows.

(a) LVRT *Mode*-5 in the *Case*-4: $P_{MD} = -60$ KW, $P_{LD} = -20$ kW, $P_{LA} = 0$, $P_{MAfb} = 80$ kW, $Q_{MA} = 0$, $|P_{LA(rated)}| = 70$ kW

(b) LVRT *Mode*-4 in the *Case*-5: $P_{MD} = -60$ KW, $P_{LD} = -20$ kW, $P_{LA} = 0$, $P_{MAfb} = 80$ kW, $Q_{MA} = 0$, $|P_{LA(rated)}| = 100$ kW

(c) LVRT *Mode*-4 in the *Case*-6: $P_{MD} = 60$ KW, $P_{LD} = -20$ kW, $P_{LA} = -90$ kW, $P_{MAfb} = 50$ kW, $Q_{MA} = 0$, $|P_{LA(rated)}| = 100$ kW.

Figure 22 shows experimental results of LVRT *Mode*-5 in *Case*-4 of power configuration under a voltage sag-depth of 0.35. In the stable-state of $N_v = 0.35$, $P_{MA(max)} = 21.3$ kW, $P_{LA(temp)} = 58.7$ kW, $P_{MA\_O^*} = 10$ kW. Since $|P_{LA(temp)}| < |P_{LA(rated)}|$ and $P_{MA\_O^*} > 0$, the PET enters into LVRT *Mode*-5, the active power absorbed from the grid P_{MA} is equal to $P_{MA\_O^*}$, which is limited and more than zero, and $P_{LA(set)}$ is equal to $|P_{LA(rated)}|$. The active-power regulation path meets that in Figure 8(a).

Figures 23 and 24 show experimental results of the LVRT *Mode*-4 in the *Case*-5 and *Case*-6 of power configuration, respectively. In Figure 23, the voltage sag-depth is 0.35, while that is 0.3 in Figure 24. Since $P_{MA\_O^*} < 0$ in these cases, the PET enters into the LVRT *Mode*-4, the active power absorbed from the grid P_{MA} is zero, and $P_{LA(set)}$ is equal to $-(P_{MD} + P_{LD})$. The active-power regulation path meets that in Figure 8(b).

In addition, in order to avoid a large sudden change in the active-power setting of the LVac-port in the process of voltage recovery, a ramp is set in the final stage of the active-power regulation path.

As shown in Figures 22(c), 23(c), and 24(c), there is a sudden increase in reactive power due to a delay in the detection of sag-depth, which is similar to the results shown in Figures 16(c) and 20(c). Moreover, even if the active power at the LVac port remains constant, a sudden increase in the grid-side voltage can cause an active power overshoot due to the inertia of the system.

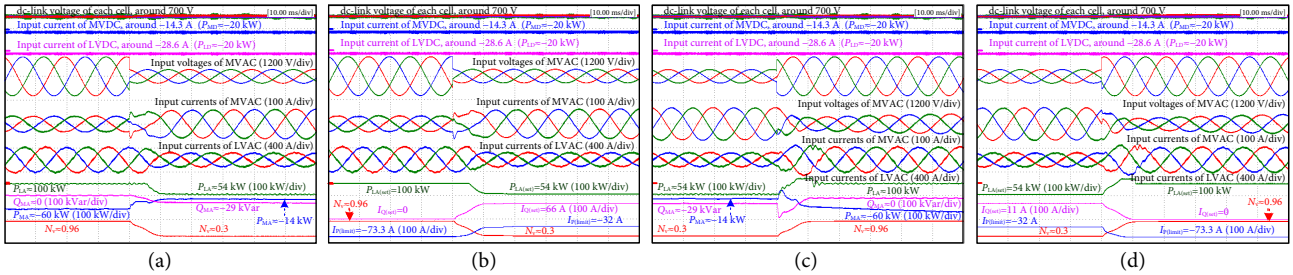

Fig. 20 Experimental results of LVRT *Mode*-1 in *Case*-3 of active-power configuration. **(a)** Real-time power curve in the voltage sag process. **(b)** Power command curve in the voltage sag process. **(c)** Real-time power curve in the voltage recovery process. **(d)** Power command curve in the voltage recovery process.

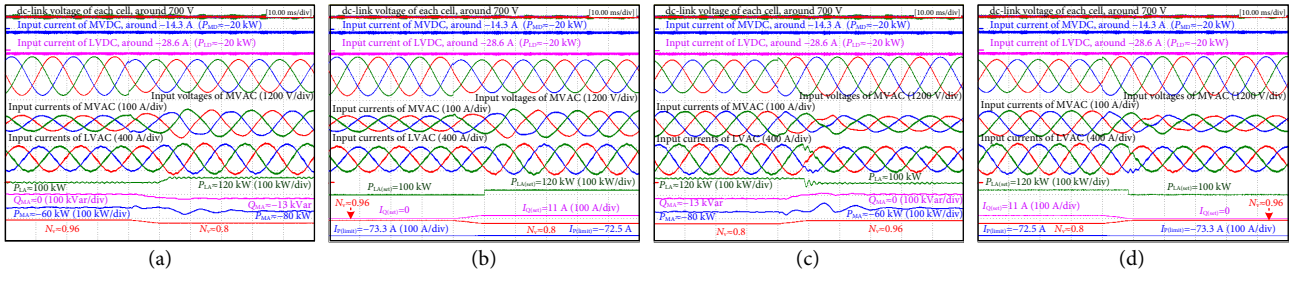

Fig. 21 Experimental results of LVRT *Mode*-2 in *Case*-3 of active-power configuration. **(a)** Real-time power curve in the voltage sag process. **(b)** Power command curve in the voltage sag process. **(c)** Real-time power curve in the voltage recovery process. **(d)** Power command curve in the voltage recovery process.

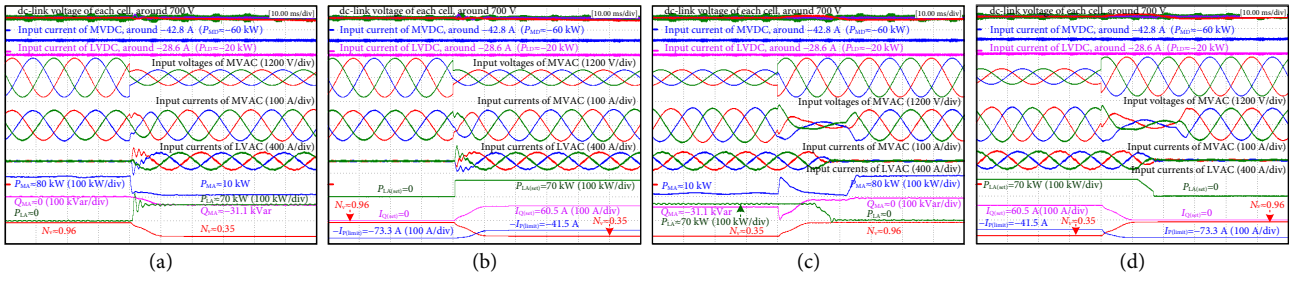

Fig. 22 Experimental results of LVRT *Mode*-5 in *Case*-4 of active-power configuration. **(a)** Real-time power curve in the voltage sag process. **(b)** Power command curve in the voltage sag process. **(c)** Real-time power curve in the voltage recovery process. **(d)** Power command curve in the voltage recovery process.

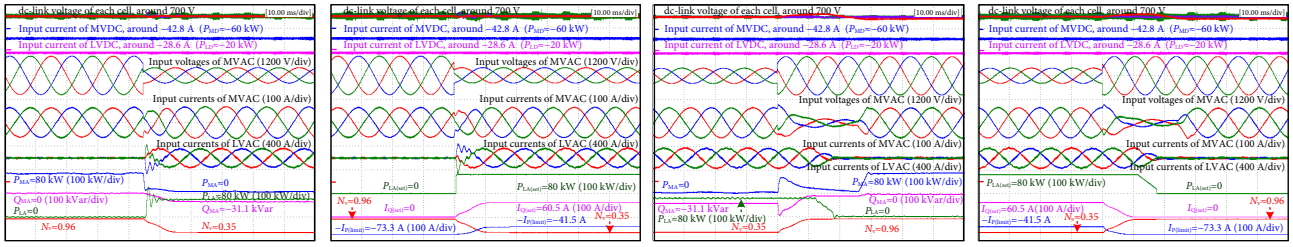

Fig. 23 Experimental results of LVRT *Mode-4* in *Case-5* of active-power configuration. (a) Real-time power curve in the voltage sag process. **(b)** Power command curve in the voltage sag process. **(c)** Real-time power curve in the voltage recovery process. **(d)** Power command curve in the voltage recovery process.

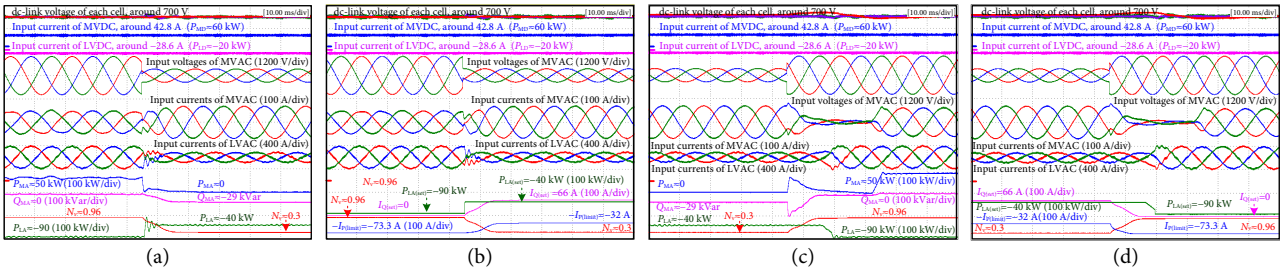

Fig. 24 Experimental results of LVRT *Mode-4* in *Case-6* of active-power configuration. (a) Real-time power curve in the voltage sag process. **(b)** Power command curve in the voltage sag process. **(c)** Real-time power curve in the voltage recovery process. **(d)** Power command curve in the voltage recovery process.

In conclusion, the response times of active power and reactive power are both 10 ms in the voltage sag process, which is indicated in Figures 22(a)–24(a). In the voltage recovery process, the reactive power is restored within 10 ms, and the response time of active power is about 30 ms. Furthermore, the input-current amplitude has never exceeded 73.3 A. Therefore, the proposed control strategy can meet the requirements of LVRT well.

6.5 LVRT performance improvement by optimizing the active-power regulation path

From Figure 20, in *Case-3* of active-power configuration, the PET enters into the LVRT *Mode-1* after the grid-voltage drops. No overcurrent occurs during the LVRT transition period while the active-power regulation is executed according to the optimized path shown in Figure 7(c). However, as shown in Figure 25, the input-current of MVac-port will exceed the limit by about 14 A if the optimized active-power regulation path is not adopted, that is, instead of remaining unchanged, the value of $P_{LA(set)}$ is adjusted based on the estimated voltage sag-depth N_v during t_1–t_2.

It is indicated that the proposed optimized path can be used to adjust the active power of PET to improve the LVRT performance.

7 Conclusions

In order to improve the reliability of HFB-PET and the toughness of the distribution grid with it as the core, an LVRT control strategy for the multi-port HFB-PET is proposed, and its main features include the following.

(a) The LVRT implementation is based on the power co-regulation of multiple ports. During the grid-side voltage sag and recovery process of the MVac port, by adjusting the grid-connected active power of the LVac port, the active powers of all the ports can be quickly rebalanced to prevent overcurrent or overvoltage. It does not require additional control

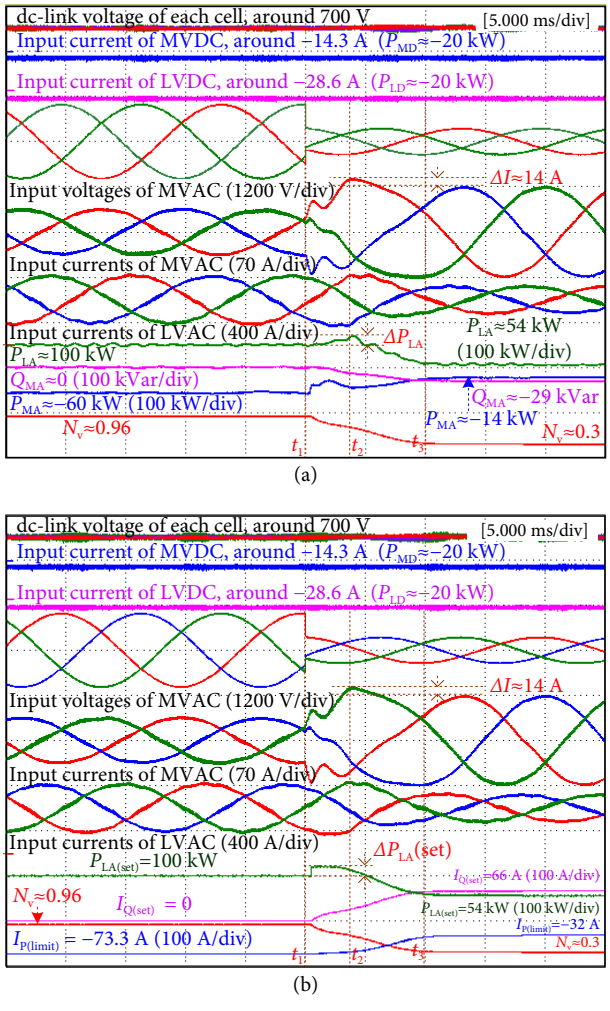

Fig. 25 Experimental results without optimized active-power regulation path. (a) Real-time power curve. **(b)** Power command curve.

to be imposed on each external DER converter connected to the HFB–PET, which reflects the relative independence of HFB–PET and external DER control.

(b) Considering grid-voltage sag-depth, port power flow and port rated capacity, etc., a classification method of LVRT modes based on the power coordinate frames is designed. Six LVRT modes are classified to meet all application scenarios, so as to the LVRT capability in both power-generation and power-consumption states for the multi-port HFB–PET.

(c) An effective and practical method for detecting the grid-voltage sag-depth is proposed. Compared with the estimation algorithm based on PLL, by adding a quadratic notch filter and a low-pass filter on the d-axis and q-axis, a larger detection bandwidth can be obtained.

(d) By optimizing the active-power regulation path during the LVRT transition period, the overcurrent issue induced by the grid-voltage sag-depth detection delay is overcome.

Finally, experimental results show that the response time of reactive power is 10 ms, and that of active power is less than 40 ms during the LVRT transition period, indicating that the proposed control strategy can meet the LVRT requirements well.

Acknowledgements

This work is supported by the National Nature Science Foundation of China (Grant No. U2034201) and the key project of Science and Technology Innovation Program of Army Engineering University (Grant No. KYCQJQZL2119). The authors would like to thank Fuji Electric Co., Ltd. for all the support to this research.

Article history

Received: 9 July 2022; Revised: 8 August 2022; Accepted: 20 August 2022

Additional information

Declaration of competing interest

The authors have no competing interests to declare that are relevant to the content of this article.

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